IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT'S MAIN BRIEF ON APPEAL
(RESUBMITTED)

APPLICANT:	Husung, et al.	DOCKET NO:	P03,0413
SERIAL NO.:	10/675,304	ART UNIT:	2614
FILED:	September 30, 2003	EXAMINER:	Dabney, Phylesha Larvinia
CONF. NO.:	5359		
TITLE:	HEARING AID DEVICE OR HEARING DEVICE SYSTEM WITH A CLOCK GENERATOR		

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Commissioner for Patents
PO Box 1450
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Sir:

This resubmitted Appeal Brief is responsive to the Notification of Non-Compliant Appeal Brief mailed June 28, 2007. The Appeal Brief was deemed to be non-compliant because the Brief does not present an argument under a separate heading for each ground of rejection on appeal. This Resubmitted Appeal Brief includes the contents of the prior Appeal Brief, with the required headings.

In accordance with the provisions of 37 C.F.R. §41.37, Appellant submits this Brief in support of the appeal of the above-referenced application in support of the patentability of claims 1-14 finally rejected in the Office Action, dated September 6, 2006. A copy of the claims on appeal is attached as Appendix A. A Notice of Appeal was filed on March 6, 2007.

REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee, Siemens Audiologische Technik GmbH, a German corporation, by virtue of the Assignment recorded February 17, 2004, at reel/frame 014978 / 0463.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and no related interferences known to Appellant, Appellant's Assignee, or Appellant's legal representative.

STATUS OF CLAIMS

Claims 1-14 are on appeal, and constitute all pending claims of the application. In the Final Office Action (FOA), in ¶1, the claims were rejected as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
1–2, 7–8 & 11–14	§102(e) Anticipation	• Pedersen (U.S. Patent Pub. No. 2004/0247148).
3–6 & 9–10	§103(a) Obviousness	• Pedersen (U.S. Patent Pub. No. 2004/0247148).

STATUS OF AMENDMENTS

Amendment D After Final was filed on February 6, 2007, following the final rejection in the September 6, 2006, Office Action. An Advisory Action was mailed on March 16, 2007, and indicated that this amendment did not place the application in a condition for allowance for a number of reasons. However, the Advisory Action was silent as to whether the amendment would be entered for purposes of appeal, with none of the item 3 or 7 boxes checked.

It is the Appellants' position that this amendment has been entered or should be entered for the following reasons. This amendment changed only one word of claim 1 from "oscillations" to "jitters" for purposes of clarity and consistency. Claim 7 had, in its original form, included a jitter unit. It is clear that the Examiner treated the structure of the jitter unit as equivalent to the method step performed by it, since the FOA, on p. 2, the Examiner stated:

> Regarding claims 1–2, they disclose the method corresponding to the apparatus claims 7–8. The method is inherent in that it simply provides the logical implementations of the structure found in claims 7–8.

Amendment D is therefore entirely consistent with the Examiner's interpretation, and simply provides additional argumentation with respect to the

declaration submitted under 37 C.F.R. §1.131 and art arguments, which are repeated herein.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The use of page and line numbers and reference characters in the drawings in the following summary is provided by way of example and is in no way intended to limit the claimed subject matter unless expressly indicated.

In general terms, many modern hearing devices comprise a digital signal processor to process incoming sound signals that have been converted to digital signals so that the signal can be processed digitally [0007]. The digital signal processor is driven by a clock generator—however, the clock frequency is not very stable due to the fact that the small size of hearing aids prohibits the use of quartz for stability [0007]. The clock generates electromagnetic noise whose signal or overtone signals can be mistakenly read by a wireless receiver as a valid signal and therefore disrupt the receiver [0008]. Although the clock generator can be designed so that its frequencies and overtones do not lie within the frequency band of the receiver, given the lack of stability of the clock, it is possible for the clock frequency or its overtones to drift over time so that they do interfere within the receiver frequency band [0008].

To address this problem, a jitter unit is provided which introduces deliberate minor frequency oscillations to the clock signal [0020]. This deliberate destabilization leads to the energy portion of the noise signals generated being divided with the clock frequency, and their harmonics are spread over a larger frequency band, and thus the frequency-specific energy is less, resulting in the amplitude of the noise signal caused by the harmonics to lie below a receiving threshold of the receiver and thus not to interfere with the receiver [0019].

Focusing on the claim language, the present invention in independent **claim 1** is directed to a method for operating a hearing aid device or hearing device system, comprising:

acquiring an input signal with at least one input transducer 1 (Fig. 1, [0022]);

transducing the input signal into an electrical signal with the input transducer ([0022]);

converting the electrical signal into a digital signal with an A/D converter 2 ([0022]);

processing the digital signal with a digital signal processing unit 3 ([0022]);

delivering an output signal with an output transducer 4 ([0022]);

generating a clock signal with a clock generator 6 to control the digital signal processing unit 3 ([0022], [0025]);

generating frequency jitters 14 in the clock signal originating from the clock generator 6 ([0025]); and

at least one of transmitting and receiving a wireless transmission12, 13 ([0024]) between the hearing aid device or hearing device system and a further device.

Claim 7 is directed to a corresponding apparatus, comprising:

at least one input transducer 1 (Fig. 1, [0022]) configured to acquire an input signal and transduce it into an electrical signal;

an A/D converter 2 ([0022]) configured to convert the electrical input signal into a digital signal;

a digital signal processing 3 ([0022]) unit configured to process the digital signal;

a clock generator configured 6 to generate a clock signal to control the digital signal processing unit 3 ([0022], [0025]);

an output transducer 4 ([0022]) and at least one of a transmitting and receiving unit 12, 13 [0024]) configured to wirelessly transmit between the hearing aid device or hearing device system and a further device; and

a jitter unit 14 associated with the clock generator 6 configured to generate frequency oscillations in the clock signal [0025]).

Claim 8 is directed to the hearing device wherein an internal clock signal of the clock generator is modulated with a further signal to generate the frequency oscillations of the clock signal ([0020]). **Claim 9** further refines claim 8 where the internal clock system is modulated with a sine signal. Similarly, **claim 10** further refines claim 8 where the internal clock system is modulated with a noise signal. **Claim 11** refines claim 8 wherein the frequency of the further signal lies above the audible frequency range. **Claim 12** refines claim 7 wherein the frequency of the clock signal oscillates around an average frequency. Finally, **claim 13** requires at least one of the transmitting unit and the receiving unit to be integrated into the hearing aid device.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues on appeal are as follows:

1. Whether the declaration under 37 C.F.R. §1.131 is sufficient to establish conception and diligence from a date prior to the filing date of the Pedersen (U.S. patent publication no. 2004/0247148) reference; and (in the alternative)

2. Whether the subject matter of claims 1-14 are anticipated under 35 U.S.C. §102 or obvious under 35 U.S.C. §103(a) in view of Pedersen.

ARGUMENT

ARGUMENT 1–Sufficiency of Declaration under 37 C.F.R. §1.131

Examiner's Position: The Applicant has not shown diligence in the completion of the invention from the time just prior to the date of the reference continuously up to the date of the filing date of the application.

In the FOA, on p. 4, the Examiner indicated that Applicants' declaration filed on March 29, 2006, under 37 C.F.R. §1.131 had been considered, but was ineffective to overcome the Pedersen reference. On p. 5, in relevant portion, the Examiner stated:

> The evidence submitted in insufficient to establish diligence from a date prior to the date of reduction to practice of the Pedersen reference to either a constructive reduction to practice or an actual reduction to practice.

> The Applicant must show diligence in the completion of the invention from the time just prior to the date of the reference continuously up to the date of the actual reduction to practice or up to the filing date of the application. Evidence of diligence must be shown for the entire critical period. If there is a long interval of unexplained inactivity, then diligence has not be [sic] established.
>
> The Applicant must show completion of the invention commensurate with the extent that the whole invention as claimed is shown by evidence. This evidence must include:
>
> 1) a statement of facts;
>
> 2) the facts must be shown in the form of sketches, blueprints, notebook entries, models, etc. for the entire critical time period;
>
> 3) all acts relied upon mush have occurred in this country or a NAFTA or WTO member country after the effective date of the Pedersen reference.
>
> [Emphasis in original]

Appellants responded in Amendment D After Final illustrating how diligence had, in fact, been shown (the details of this response are discussed below). In the Advisory Action mailed March 16, 2007, the Examiner stated that disallowing the declaration is proper, articulated the three ways in which an applicant can establish prior invention pursuant to 37 C.F.R. §1.131, and stated:

> The effective filing date for the Pedersen reference is 9/20/02. As per the requirements for 37 CFR 1.131 one of the sections would need to be satisfied. Sections A, B, or C were not satisfied since the Applicant failed at least one portion of the requirement, namely diligence is not met since there is a lapse in time between 5/22/02 and 9/30/02 where nothing was recorded for constructive reduction to practice.

Appellant's Position: The activities of the Appellant demonstrate conception and diligence from a time prior to the filing date of the Pedersen reference to constructive reduction to practice (filing of the application).

In the previously submitted Amendment C, mailed March 24, 2006, the

Applicants submitted an inventor declaration under 37 CFR §1.131 to establish conception and diligence prior to the date of the Pedersen reference. Pedersen was filed as a PCT application on September 20, 2002 (with Appellants noting that Pedersen's priority date is of no consequence under 35 U.S.C. §102(e)).

The declarations of Kunibert Husung and Torsten Niederdränk were filed that established:

Conception of the invention prior to the September 20, 2002, filing date of Pedersen

- conception by the inventor prior to May 3, 2002;

Diligence of the inventor in from a time just prior to the date of the reference continuously up to the date of the filing date of the application

- conception documented in invention disclosure report;
- invention disclosure report executed by inventor on May 3, 2002;
- invention report submitted to Siemens patent manager;
- invention report accepted and signed by patent manager on May 14, 2002;
- invention report submitted to Siemens Patent Department;
- invention report registered in the Siemens Patent Department on May 22, 2002;
- application filed in Germany (priority application) on September 30, 2002.

The Appellants did provide: 1) a statement of facts (Kunibert Husung and Torsten Niederdränk declarations); 2) facts shown in the form of sketches, etc. (the invention disclosure report) for the entire critical period (the time of creating and executing the invention report on May 3, 2002, through the filing of the application on September 30, 2002; and 3) all acts relied upon occurred in Germany, which is a WTO member country.

The difficulty in the present case in hand is that the Pedersen reference was filed on September 20, 2002, whereas the priority application was filed on September 30, 2002. This leaves only ten days in between.

Appellants note that the Examiner's primary basis for deeming the

declaration insufficient is due to the lapse in time between 5/22/02 and 9/30/02. Thus, the specific issue before the Board is whether diligence has not been shown when there is a lack of evidence showing activity for a period of just over four months prior to the filing date.

Although the Appellants provided a reasoned basis as to why the documented activities from conception to constructive reduction to practice do, in fact, demonstrate diligence, the Examiner simply provided a conclusory statement that an absence of activity for just over four months failed to demonstrate diligence and did not contain any discussion addressing the merits of the Appellants' arguments. The Appellants' arguments are repeated below for consideration by the Board.

The preparation of a patent application suitable for filing is an involved and complex process. It involves a coordination between the inventors, draftsmen and patent attorneys, agents, and/or patent professionals to annotate drawings, develop proper claim scope, review prior art documents, finalize the application, and getting authorization to file the application. A four month time period for this type of activity for a large multi-national corporation, following the clearly documented level of activity occurring between May 3, 2002, and May 22, 2002, does not constitute a "long interval of unexplained inactivity", but rather is what one would come to expect as a natural time period for activities necessary to bring an invention disclosure to its ultimate fileable form.

The period of just over four months is not an excessive period of time for a large multinational corporation who is developing many patent disclosures into applications for filing, given the extensive preparations that are required for bringing an invention disclosure into fileable form, as described above.

The fact that there are not daily memos documenting the activities related to this application from September 19, 2002, (the day immediately before the filing date of Pedersen) to September 29, 2002, (the day immediately before the filing date of the present priority document) does infer that there is a long interval of unexplained inactivity and does not serve to destroy the establishment of

diligence.

For these reasons, the Appellants respectfully contend that the evidence of record *does* adequately establish an earlier conception date and a showing of diligence from prior to the filing date of the Pedersen reference to the point of constructive reduction to practice.

However, in the event that this showing is still deemed to be inadequate, the Appellants have provided below, in the alternative, a technical basis for distinguishing the Pedersen reference on the merits.

ARGUMENT 2–Anticipation and Obviousness of Claims 1, 7, and 14 in View of Pedersen

Examiner's Position: Pedersen anticipates claims 1 and 7 because it teaches each and every element of these claims. Pedersen's phase-locked-loop (PLL) teaches a jitter unit or a unit to generate frequency oscillations in the clock signal.

In the FOA, on p. 2, the Examiner indicated that claims 1 and 2 disclose a method corresponding to the apparatus claims 7 and 8, in that the method is inherent because it simply provides a logical implementation of the structure found in claims 7 and 8. The Examiner's analysis then focused on apparatus claims 7 and 11–13.

On pp. 2–3, the Examiner indicated how each of the elements of independent claim 7 was taught by Pedersen. Significantly, the Examiner pointed to Pedersen's PLL, discussed in paragraph 0093, as reading on the claimed jitter unit associated with the clock generator configured to generate frequency oscillations in the clock signal.

With regard to claim 14, the Examiner stated, on p. 3, that Pedersen teaches a remote unit for storing additional programs, which reads on there being at least one of a further external transmitting/receiving unit connected with the further hearing device.

Appellants' Position: Claims 1, 7, and 14 are not anticipated by Pedersen because Pedersen fails to teach or suggest all elements of claims 1, 7, and 14. Most importantly, Pedersen's PLL cannot be used to read on the jitter

unit / oscillator as claimed by the independent claims of the application. Pedersen implicitly teaches away from the invention by a teaching of stabilizing the clock signal, whereas the present invention destabilizes it.

Claims 1, 7, and 14 are not anticipated by Pedersen because Pedersen fails to teach or suggest all elements of the independent claims. Most importantly, Pedersen's PLL cannot be used to read on the jitter unit / oscillator as claimed by the independent claims of the application. Pedersen implicitly teaches away from the invention by a teaching of stabilizing the clock signal, whereas the present invention destabilizes it.

The jitter unit 14, as claimed in the present invention, has an exact opposite effect as the PLL disclosed in Pedersen. In Pedersen, the PLL is used to stabilize the clock signal, whereas the jitter unit / oscillator of the present invention is used to *destabilize* the clock signal, with very differing purposes and effects.

The present invention deals with the problem of reducing an electromagnetic interference signal that is generated and emitted by a hearing device due to its clocked operation. Pedersen deals with a very different problem, which is the optimization of the power consumption in a hearing device. Pedersen proposes, among other things, that the clock frequency can be decreased to save power.

In the present invention, the destabilization of the clock signal (via the jitter mechanism) leads to the situation that both: 1) the energy portions of the interference signals generated in the hearing aid device being distributed with the clock frequency, and 2) their harmonics being distributed on a larger frequency band, and therewith, the frequency-specific energy is reduced.

This, in turn, means that the amplitude or an interference signal caused by the harmonics lies below the reception threshold of the reception unit given a correspondingly-dimensioned fluctuation of the clock signal. Harmonics of the clock frequency therefore no longer lead to interferences given wireless reception of a signal from an external device. In general, this is advantageous in that a hearing aid device in connection with a signal transmission system for wireless

signal transmission enables an interference-free communication.

The clock frequency in the invention remains (in a broad, general sense) unchanged, in contrast to Pedersen, whereby the clock frequency is adjusted corresponding to the requirements and then remains unchanged at least over a longer time span. When the clock frequency is changed (for example reduced) in Pedersen, this means that the time interval between two clock edges is always larger. This is not the case in the invention. There the time interval between two clock edges should always remain constant, on average, over a longer time span.

Of some significance, the Examiner stated, in the OA on p. 3 that Pedersen discloses a jitter unit (PLL, paragraph 0093) associated with the clock generator configured to generate frequency oscillations in the clock signal. As described in the specification of the present application, paragraphs [0017]–[0020], the jitter unit performs a function of *destabilizing* the clock signal. A stable clock signal is modulated with a further signal to produce the destabilized clock signal.

In the Advisory Action, the Examiner asserted that the features upon which the applicant relies (i.e., stability versus instability of the signal) are not recited in the rejected claims, stating that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

While the Appellants acknowledge that the Examiner is permitted to give claim terms their broadest reasonable interpretation (MPEP §2111), this interpretation must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright,* 165 F.3d 1353, 1359 (Fed. Cir. 1999), cited in MPEP §2111. The words of a claim must be given their plain and ordinary meaning, which means the ordinary and customary meaning given to the term by those of ordinary skill in the art. MPEP §2111.01.

It is well known in the art that PLL is a closed-loop feedback control system that generates and outputs a signal in relation to the frequency and phase of an input (“reference” signal), and automatically raises or lowers the frequency of a controlled oscillator unit until it is matched to the reference in both frequency

and phase—it is used where it is desired to stabilize a generated signal.

This well-known usage is consistent with how Pedersen applies it. Pedersen states, in paragraph [0093], "The clock frequency of the DSP itself may be controlled by an analogue or digitally-controlled circuit, e.g., a phase locked loop PLL." Although Pedersen's PLL is used in a slightly more complex manner (driving the DSP by a programmable control PLL-based multiplication circuit), the overall purpose is stability of the DSP clock frequency. Clearly the PLL of Pedersen does not serve to *destabilize* the clock signal and deliberately introduce frequency variation, and therefore, it is improper for the Examiner to apply Pedersen's teaching of the PLL circuit as reading on the jitter unit according to the present invention.

Claim 7 requires the element of a jitter unit associated with the clock generator configured to *generate* frequency oscillations in the clock signal. The PLL of Pedersen is configured to *remove* or *stabilize* frequency oscillations in the clock signal. Although the Examiner is permitted to broadly construe the term "jitter unit" in the present invention, it is impermissible for the Examiner to stretch that claim language to be so broad as to cover a concept that is opposite to that which is well known to those of ordinary skill in the art. It is well known that a jitter is an abrupt variation of signal characteristics, such as the interval between successive cycles or the frequency or phase of successive cycles. The ordinary meaning of this term describing a destabilizing characteristic cannot be read on by disclosed structure describing a stabilizing characteristic. Thus, Pedersen's discussion of the PLL structure that serves to stabilize is an implicit, even if it is not an explicit, teaching away of the principle of the jitter unit that serves to destabilize in the present invention. The Examiner cannot ignore disclosure that teach away from the claims (MPEP §2141.02(VI)).

Nor can the proposed modifications change the principle operation of a reference (MPEP §2143.01(VI))—the principle of operation of the present invention is a destabilization of the clock signal (via the jitter unit). The principle of operation of Pedersen's invention is the stabilization of the clock signal (via the

PLL). The Examiner, by reading Pedersen's PLL on the jitter unit of the present invention, has thus impermissibly attempted to use the Pedersen reference to change the principle of operation of the present invention as claimed.

This distinction is further highlighted when looking to the features of the dependent claims in the application. The Examiner dismisses a number of the dependent claims as either being anticipated or obvious over Pedersen because, "it is known for PLL circuits to produce modulated signals of any wave pattern" (p. 4).

Appellants contend that it is known for PLL circuits to *utilize* signals of any wave pattern as *reference signals*, but the output of a PLL, as known by those of ordinary skill in the art, is a signal that reflects a deviation from a source signal and the reference signal.

ARGUMENT 3–Anticipation of Claims 2 and 8 in View of Pedersen

Examiner's Position: Pedersen anticipates claims 2 and 8 because it teaches an internal clock signal of the clock generator that is modulated with a further signal to generate the frequency oscillations of the clock signal.

With regard to claim 8 (and claim 2), on p. 3, the Examiner indicated that the internal clock signal of the clock generator is modulated with a further signal (produced by the PLL, paragraph 0093) to generate the frequency oscillations of the clock signal.

Appellants' Position: Claim 2 and 8 are not anticipated by Pedersen because Pedersen fails to teach or suggest all elements of claims 1 and 7 from which claims 2 and 8 respectively depend. It would not be known from the teaching of Pedersen's PLL to have a PLL modulate the clock generator with a further signal to generate frequency oscillations of the clock signal.

Regarding **claim 8**, it would not be known from the teaching of Pedersen's PLL to have a PLL modulate the clock generator with a further signal to generate frequency oscillations of the clock signal. As noted above, the purpose of a PLL is to remove frequency oscillations from a clock signal.

ARGUMENT 4–Anticipation of Claims 11–13 in View of Pedersen

Examiner's Position: The Examiner has not presented a position with regard to the features of dependent claims 11–13.

With regard to claims 11–13, the Examiner is silent as to how the further frequency signal lies above the audible frequency range (claim 11), how the frequency of the clock signal oscillates around an average frequency (claim 12), and how the transmitting unit and/or the receiving unit are integrated into the hearing aid device (claim 13).

Appellants' Position: The Examiner has not sustained a prima facie case of obviousness given a complete lack of any discussion pertaining related to the limitations of dependent claims 11–13.

With regard to **claims 11–13**, given that the Examiner has provided absolutely no discussion as to how the further frequency signal lies above the audible frequency range (claim 11), how the frequency of the clock signal oscillates around an average frequency (claim 12), and how the transmitting unit and/or the receiving unit are integrated into the hearing aid device (claim 13), the Appellants respectfully assert that the Examiner has failed to establish a prima facie case of obviousness with respect to these claims.

ARGUMENT 5–Obviousness of Claims 3, 4, and 9–11 in View of Pedersen

Examiner's Position: It would have been obvious for one of ordinary skill in the art to use any wave pattern, such as a sine wave pattern, in the invention of Pedersen for improving the clock signal

On pp. 3–4, the Examiner applied an obviousness standard to claims 3–6, 9, and 10, observing that claims 3–6 disclose a method corresponding to the apparatus claims 9–12, noting that the method is inherent in that it simply provides the logical implementation of structure found in claims 9–12.

With regard to claim 9, the Examiner stated, on p. 4, that although Pedersen does not specifically teach that the internal clock system is modulated with a sine signal, it is known for PLL circuits to produce a modulated signal of any wave pattern for beneficially adjusting the signal of the clock up and down,

and therefore, it would have been obvious for one of ordinary skill in the art to use any wave pattern, such as a sine wave pattern, in the invention of Pedersen, for improving the clock signal.

With regard to claim 10, the Examiner similarly observed that Pedersen does not teach that the clock system is modulated with a noise signal, but noted that it is known for PLL circuits to produce a noise signal and to beneficially control this noise signal for increasing or decreasing the amount of jitter. The Examiner concluded that it would have been obvious to one of ordinary skill in the art to use the noise signal produced by the PLL circuit of Pedersen to increase or decrease the amount of jitter produced.

In responding to the Appellants' Amendment after final, the Examiner stated:

> With respect to the Applicant arguments pertaining to the different problems being solved between the Applicant and Pedersen, it is noted that the features upon which the applicant relies (i.e., stability versus instability of the signal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. [citation omitted].

Appellants' Position: A PLL, which the Examiner has equated with the claimed jitter unit, cannot be used to modulate a signal with any specific characteristic outside of its role of creating a phase-locked loop, and therefore, it would not be obvious to one of ordinary skill in the art to use the teaching of Pedersen to teach or suggest using the PLL to modulate the clock signal with a sine signal, noise signal, or with a frequency above any particular predefined value.

A PLL, which the Examiner has equated with the claimed jitter unit, cannot be used to modulate a signal with any specific characteristic outside of its role of creating a phase-locked loop, and therefore, it would not be obvious to one of ordinary skill in the art to use the teaching of Pedersen to teach or suggest using the PLL to modulate the clock signal with a sine signal, as claimed in claim 9, a noise signal, as claimed in claim 10, or with a frequency above any particular predefined value, as claimed in claim 11. It would make no sense to use a PLL in

such a manner if its role is to create a phase-locked loop. One of ordinary skill in the art would not utilize Pedersen's PLL in such a manner, as it would make no sense to do so.

For the above reasons, Appellants respectfully contend that none of the claims of the present invention are anticipated nor obvious in view of the disclosure of Pedersen.

CONCLUSION

For the above reasons, Appellants respectfully submits that the Examiner is in error in law and in fact in rejecting claims 1–14 based on the teachings of Pedersen. Reversal of the rejection of all of those claims is justified, and the same is respectfully requested.

The previous Appeal Brief was accompanied by an authorization to charge the Applicants' representative's credit card in the amount of $500.00, as required by 37 C.F.R. §41.20(b)(2). It is believed that no additional fee is due for this Resubmitted Brief. However, if necessary, the Commissioner is hereby authorized to charge any additional fees which may be required to or credit any overpayments to account No. 501519.

Respectfully submitted,

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APPENDIX A
CLAIMS INVOLVED IN THE APPEAL

1. (previously presented) A method for operating a hearing aid device or hearing device system, comprising:

acquiring an input signal with at least one input transducer;

transducing the input signal into an electrical signal with the input transducer;

converting the electrical signal into a digital signal with an A/D converter;

processing the digital signal with a digital signal processing unit;

delivering an output signal with an output transducer;

generating a clock signal with a clock generator to control the digital signal processing unit;

generating frequency jitters in the clock signal originating from the clock generator; and

at least one of transmitting and receiving a wireless transmission between the hearing aid device or hearing device system and a further device.

2. (original) The method according to claim 1, further comprising modulating an internal clock signal generated by the clock generator with a further signal to generate the frequency oscillations.

3. (original) The method according to claim 2, wherein the internal clock signal is modulated with a sine signal.

4. (original) The method according to claim 2, wherein the internal clock signal is modulated with a noise signal.

5. (original) The method according to claim 2, wherein the frequency of the further signal lies above an audible frequency range.

6. (original) The method according to claim 1, wherein the frequency of the clock signal oscillates around an average frequency.

7. (original) A hearing aid device or hearing device system, comprising:

at least one input transducer configured to acquire an input signal and transduce it into an electrical signal;

an A/D converter configured to convert the electrical input signal into a digital signal;

a digital signal processing unit configured to process the digital signal;

a clock generator configured to generate a clock signal to control the digital signal processing unit;

an output transducer and at least one of a transmitting and receiving unit configured to wirelessly transmit between the hearing aid device or hearing device system and a further device; and

a jitter unit associated with the clock generator configured to generate frequency oscillations in the clock signal.

8. (original) The hearing aid device or hearing device system according to claim 7, wherein an internal clock signal of the clock generator is modulated with a further signal to generate the frequency oscillations of the clock signal.

9. (original) The hearing aid device or hearing device system according to claim 8, wherein the internal clock system is modulated with a sine signal.

10. (original) The hearing aid device or hearing device system according to claim 8, wherein the internal clock system is modulated with a noise signal.

11. (original) The hearing aid device or hearing device system according to claim 8, wherein the frequency of the further signal lies above the audible frequency range.

12. (original) The hearing aid device or hearing device system according to claim 7, wherein the frequency of the clock signal oscillates around an average frequency.

13. (original) The hearing aid device according to claim 7, wherein at least one of the transmitting unit and the receiving unit is integrated into the hearing aid device.

14. (original) The hearing device system according to claim 7, further comprising a further hearing aid device and at least one of a further external transmitting unit and receiving unit connected with the further hearing aid device.

APPENDIX B
EVIDENCE APPENDIX

There is no additional evidence entered and relied upon for this appeal.

APPENDIX C
RELATED PROCEEDINGS APPENDIX

There are no related proceedings associated with this appeal